SAMSUNG

IR Drop-Aware PDN Design Methodology for HBM Proxy Package Si-Interposer with 3D-IC Platform

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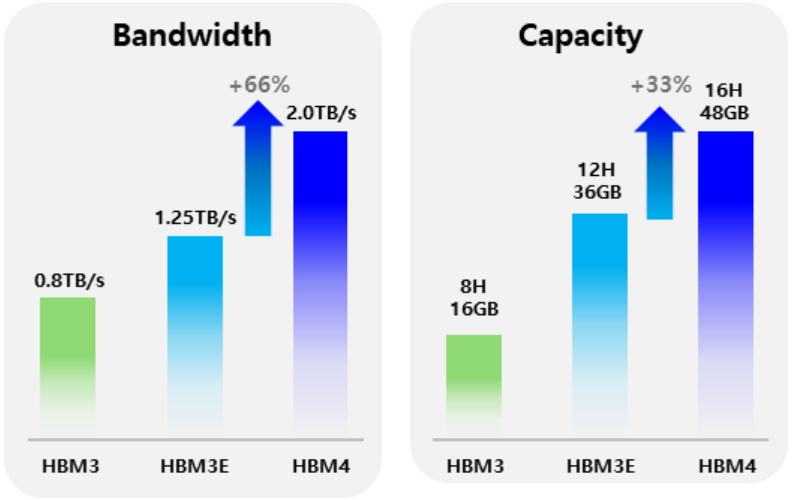
Motivation

Motivation (1) : Necessity of Power Delivery Network(PDN) Auto Routing

- The increasing design complexity of 2.5D Si-Interposer due to the growing number of AI parameters, led to the necessity of 2.5D packaging using Multi-HBM
- **As over 12,000 uBumps** are present in a single HBM4, manual routing is difficult to handle the increasing design complexity
- It is difficult to modify the PDN design that **reflects the results of multi-physics analysis**

Motivation (2) : Necessity of 2.5D Packaging System-Level IR Drop Co-Analysis

- As the power supply voltage decreases and the number of signals increases about 4000, the impact of SSN becomes greater
- **System-level co-analysis is needed** for system-level design co-optimization, since it is difficult to improve the PDN Design Quality with a single component



[Figure 1] Development of HBM

Challenges

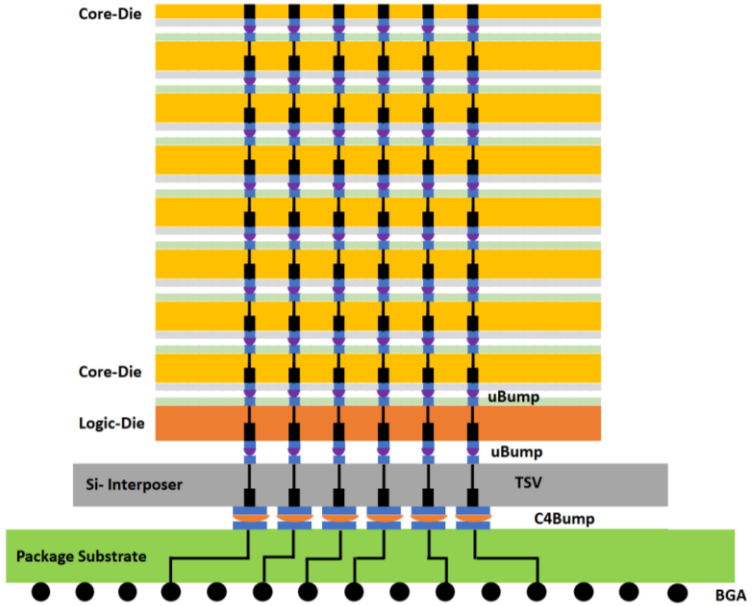
Challenges : A new methodology for designing HBM4 proxy PKG 2.5D Si-interposer PDN

(1) Absence of Si-Interposer PDN Auto Routing

- Over 20,000 bumps(uBump & C4Bump), including 450+ signals

(2) Absence of a 2.5D Packaging System-Level IR Drop Flow with HBM Collaterals (CPM)

(3) Absence of a single platform that enables efficient IR Drop-aware PDN design



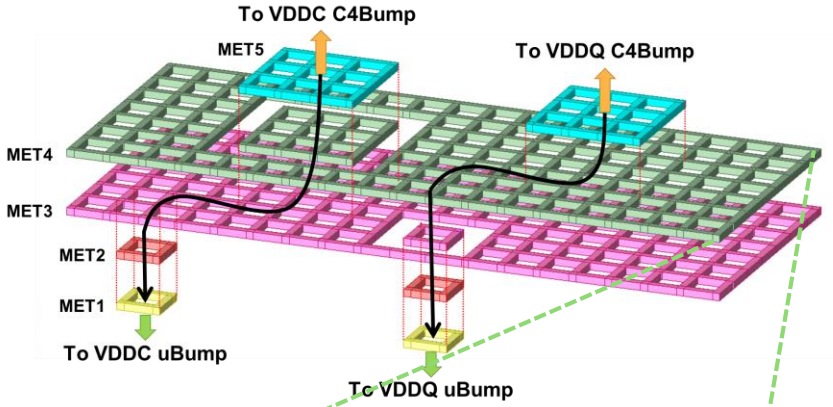
[Figure 2] HBM Proxy PKG Structure

Main Idea (1) : PDN Auto Routing

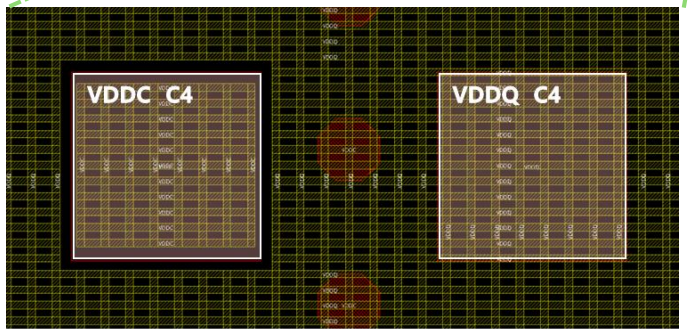
(1) PDN Auto Routing: Si-Interposer PDN Auto Routing using Innovus

- Each power is allocated and routed for each layer based on design variables
  - 5 Power / Mesh-type PDN / 5 Layer / 20,000+ bumps (uBump: 12,000+, C4Bump: 7000+)
  - Design variables: Bump Assign, Bump Pitch, Metal Width, Metal Pattern, etc.

achievement) PDN Design is performed within 3 hours.



[Figure 3] PDN Design Structure



[Figure 4] PDN Design Layout

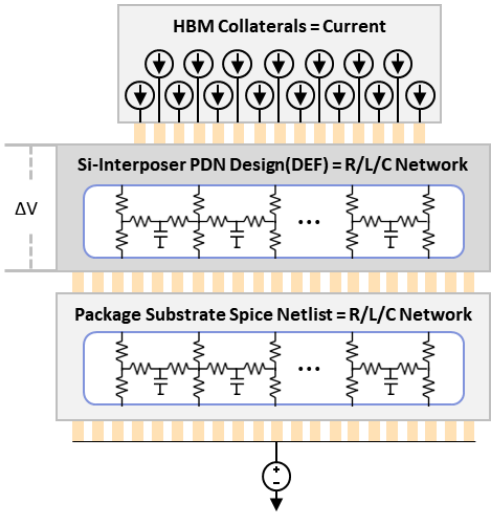
Main Idea (2) : System Level IR Drop

(2) System Level IR Drop: Si-Interposer-PKG IR Drop Co-Analysis flow using Voltus-Sigrity Package Flow

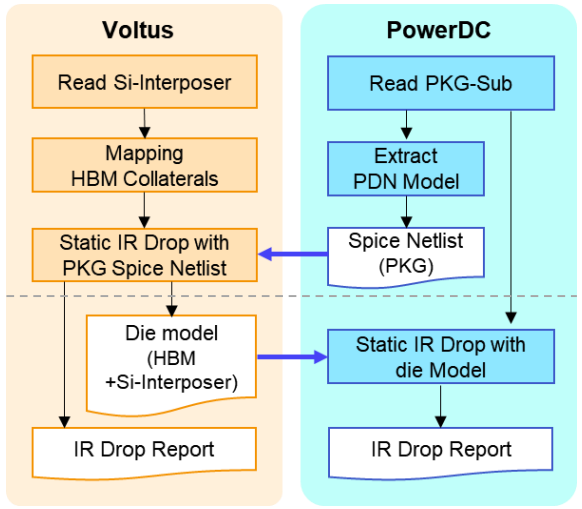
- When analyzing the IR drop of Si-Interposer using Voltus, Package Substrate PDN Spice Model extracted by PowerDC is attached to analyze it as system level
  - Whether to include the Package Substrate Spice Model in the analysis is optional
- Static IR drop is analyzed by distributing sum of HBM Current equally to each uBump of the Si-Interposer

$$Per\ uBump\ Current\ = \frac{Sum\ of\ HBM\ Current\ per\ Power\ Net}{\#\ of\ uBump\ per\ Power\ Net}$$

achievement) It is possible to evaluate the PDN Quality at the system level.



[Figure 5] 2.5D PKG Structure



[Figure 6] Voltus-Sigrity Package Flow

Main Idea (3) : 3D-IC Platform

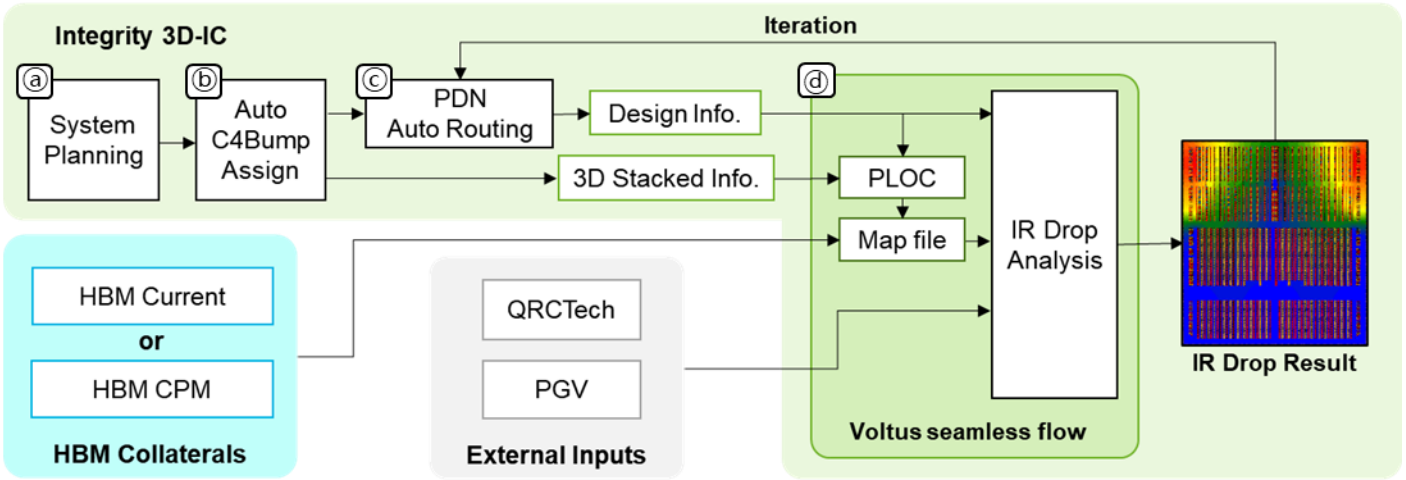
(3) 3D-IC Platform: IR Drop-Aware PDN Design Methodology with integrity 3D-IC

ⓐ System planning of 2.5D Packaging structures

- Generate 3D structural information for HBM Proxy PKG.
- Create layer stack-up information for each component.

ⓑ Auto C4bump assignment

- Update the physical information(power net, coordination, layer) of uBumps and C4Bumps.
- Assign the same power net of the nearest C4bump to the uBump's power net based on the uBump's coordinates.



[Figure 7] IR Drop-Aware PDN Design Methodology

ⓒ PDN Auto Routing using Innovus

- Perform PDN Auto Routing by reflecting the design variables (Bump Assign, Bump Pitch, Metal Width, Metal Pattern, etc.).

ⓓ IR drop analysis using Voltus seamless flow

- Under Voltus seamless flow, we could connect Si-Interposer(DEF, PDN Auto Routing result) to other components(HBM Collaterals, package substrate) and perform IR Drop.
  - ⓓ-1) Extract physical connection information for each component from Integrity 3D-IC Platform to PLOC file.
  - ⓓ-2) Creates a mapping file that connects HBM and Si-Interposer based on HBM Collaterals (HBM Current: Per uBump Current / HBM CPM: Per B-die Pad info).
  - ⓓ-3) Run Si-Interposer IR Drop Analysis on Voltus.

achievement) A new methodology has been developed for designers to efficiently design Si-Interposer PDN on a single platform.

Evidence

Challenge 1) Absence of Si-Interposer PDN Auto Routing

Challenge 2) Absence of System-Level IR Drop Flow

(1) HBM4 Si-Interposer PDN Auto Routing Runtime: < 3 hours

- The PDN Auto Routing runtime has been shortened, enabling design iterations that reflect the results of Multi-physics analysis including IR Drop analysis

(2)-1 HBM4 Si-Interposer PDN Design Quality Improvement

; 68.0% : compared to HBM3E Si-Interposer

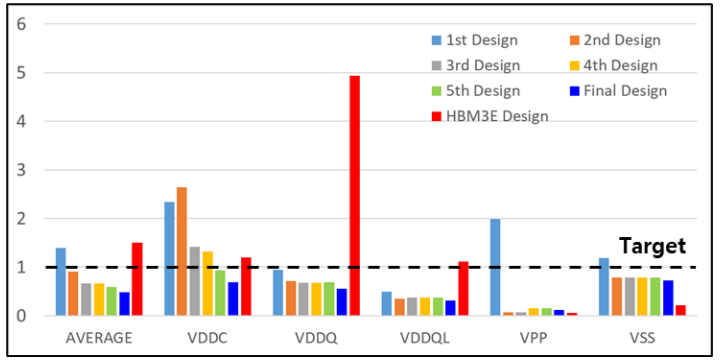
; 65.5% : compared to HBM4 1st Auto Routed PDN Design

- Iteration of PDN Auto Routing undergoing optimization of C4 bump assignment and modification of other design variables improves Si-Interposer PDN quality

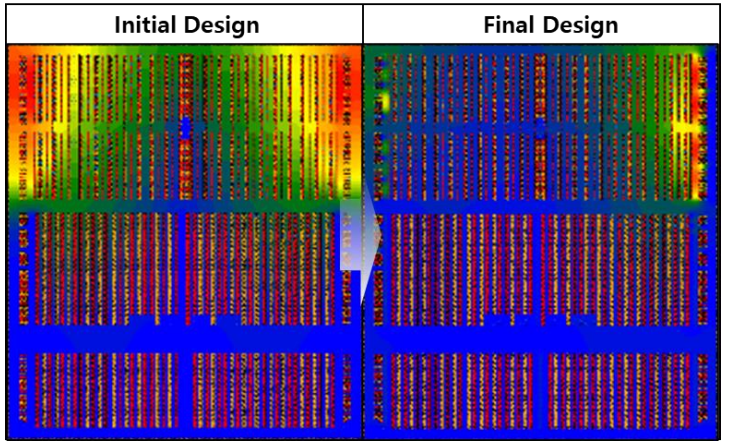
(2)-2 Si-Interposer-PKG System Level IR Drop Results Improvement: Max 56%

- Based on the system level IR drop results, we modified the discontinuous layout pattern of package substrate to achieve optimization from a system-level perspective

Analysis Condition: IDD4R / Static (Sum of HBM Current)



[Figure 8] Si-Interposer IR Drop Flow



[Figure 9] Si-Interposer IR Drop Map of VPP Net

Evidence

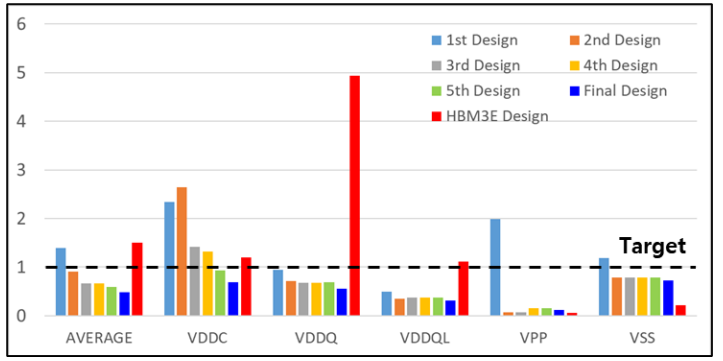
(3)-1 C4 Bump Fix & PDN Design TAT Reduction: 53%

- Applying a new PDN Design Methodology on a single platform reduced design time compared to manual routing

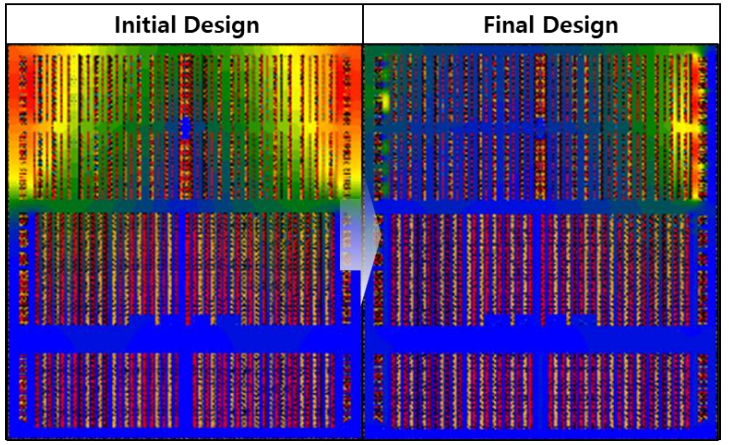
(3)-2 Design Decision: # of Layers → Manufacturing TAT & Cost : Reduction

- Through analysis of IR drop results in the early stage (diff < 1mV), we decided to change number of layers

Analysis Condition: IDD4R / Static (Sum of HBM Current)



[Figure 8] Si-Interposer IR Drop Flow



[Figure 9] Si-Interposer IR Drop Map of VPP Net

Summary

Challenge 1) Absence of Si-Interposer PDN Auto Routing

Challenge 2) Absence of System-Level IR Drop Flow

Challenge 3) Absence of a single platform

■ **Applying the IR Drop-Aware Si-Interposer PDN Design Methodology, we are able to optimize the design for the HBM4 Proxy PKG**

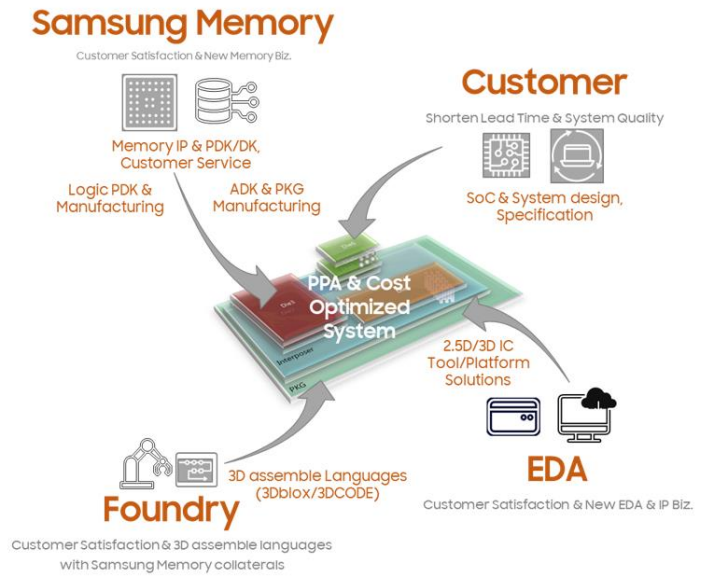
(1) We developed a new Si-Interposer **PDN Auto Routing**. The HBM4 Si-Interposer PDN Auto Routing **runtime** has been reduced **to less than 3 hours**, allowing for faster design iterations that incorporate Multi-physics analysis results, including IR Drop analysis.

(2) With the newly established **2.5D Packaging System-Level IR Drop Analysis Flow**, we were able to analyze the IR drop of the automatically routed PDN in the early stage. Through fast iterations focusing on IR Drop using PDN Auto Routing in (1), **the PDN quality** of HBM4 Si-Interposer has been **improved by Avg. 68.0%** compared to HBM3E Si-Interposer and **Avg. 65.5%** compared to HBM4 1st Design. **IR Drop co-analysis results** with Si-Interposer and Package Substrate improved by a **Max. 56%** compared to the 1st design.

(3) By integrating (1) and (2) into the 3DIC, we have developed **a new methodology to efficiently design PDNs**. This led to a **53% reduction** in **total PDN Design TAT** from C4Bump assign to C4bump fix. Furthermore, we made design decisions to reduce the number of layers in the early stage, resulting in **reduced manufacturing TAT and cost**.

Future work

- **Extendable to multi-physics solutions for System IR-drop and Power Integrity with 3D-IC Platform for hyperscalers**
  - ‘Seamless design flow’ with 3D-IC platform based on HBM Core/Logic die, Proxy Interposer, and Package co-design flow will be enabled
  - Samsung Memory in the name of STCO(System Tech Co-optimization) will provide open innovation Ecosystem to expand customers business
    - Samsung Memory will provide deliverables for customer 2.5D/3D IC system design including ‘Samsung HBM’
  - Collaborate to develop the design standards with ‘state-of-the-art’ solutions of EDA, Foundries
    - Tool, Collaterals, Flows and Design Methodologies



[Figure 10] Open Innovation Ecosystem

AI

Security

Systems

Q&A

EDA

Design

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